Design and Implementation of a Simple Moving Average Filter for a UWB/UHF Hybrid RFID Tag

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***Abstract*—The recent development of the IoT systems demands energy-efficient circuits capable of prolonged battery operation. To address this demand, a variety of circuits have been proposed to reduce the power consumption in these systems. A promising approach is to maximize the local processing with a suitable DSP module, such as a processor, to conserve energy by transmitting less data. In this work, a Simple Moving Average (SMA) filter was proposed for preprocessing signals acquired from the sensors and preparing them for further processing in the processor. With this solution, the processor can receive the preprocessed information and no longer needs software to noise reduction. The filter was validated using an FPGA and implemented using CMOS 0.18 um technology. The filter achieved a power consumption of 1.71 μW when operating with a 125 kHz clock frequency. These results show the potential of the filter to efficiently reduce noise while effectively managing power consumption in IoT systems, thereby contributing to the realization of energy-efficient designs.**

I. Introduction

The latest generation of IoT(Internet of Things) systems has an increasing demand for enhanced power efficiency. These systems are required to acquire data from sensors and process them before transmitting them to the cloud with minimal noise interference. Due to their prolonged operational requirements, these devices frequently rely on battery power. A study by [1] and [2] demonstrated that a system powered by a button cell battery needs a power consumption in the order of μW to ensure uninterrupted operation over a duration range from one to ten years.

The adoption of energy harvesting has been explored as a potential solution to address the challenges associated with power efficiency [3]. However, this approach presents its own challenges. Notably, there is a threshold below which ambient energy cannot be effectively harvested, which leads to an unstable power source unless energy is derived from an artificial source such as a WiFi access point. Therefore, a viable technique involves combining energy harvesting with battery utilization. This hybrid approach not only ensures the reliability of the battery as a power source but also harnesses the inherent benefits of energy harvesting for the system [1].

In this context, an innovative UHF/UWB(Ultra High Frequency/Ultra Wide Band) RFID(Radio Frequency Identification) tag has been developed at the University of Brasilia, incorporating a hybrid energy harvesting and battery-powered system. This system, known as Cedro Project, is an integrated

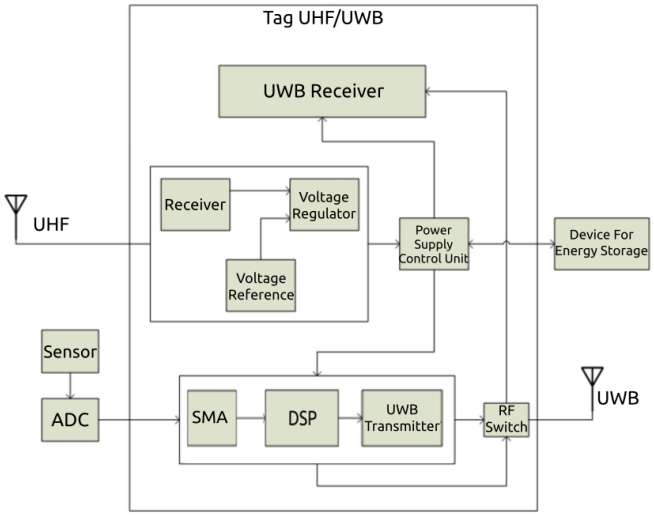

Fig. 1. Block diagram of Cedro Project architecture.

circuit aimed to enable sensor monitoring and data transmission via UWB technology. The versatility of this system allows for monitoring a diverse range of variables and offers the advantage of wireless data transmission without the need for a power plug. Furthermore, UWB communication provides notable advantages, such as reduced power consumption and the potential for high data rates, by using ultra-short pulses for data transmission and reception, operating at a nanosecond time scale [4]. In addition, this form of communication does not need a sine-wave carrier and does not require IF processing since it operates at baseband.

The system architecture is depicted in Figure 1. The key components are an UHF energy harvesting module responsible for acquiring energy from the UHF antenna; a power supply control unit, which will manage the energy from both the energy harvesting module and the battery; a UWB receiver and a UWB transmitter; an RF switch that determines the system mode (transmission or reception through the UWB antenna), and a DSP(Digital Signal Processor) module. The data received from the sensor are converted from analog to digital and then are digitally processed in the DSP block. After that, the UWB transmitter sends the processed data to an RFID

reader.

In order to address the low power requirements, a key objective is to reduce the volume of transmitted data by maximizing local processing within the DSP module. A potential approach involves developing a microarchitecture specifically tailored for digital signal processing tasks while ensuring energy efficiency. The open-source instruction set architecture (ISA) RISC-V is a suitable option, since it allows optimization and customization through application-specific instructions [5].

The goal of this work is to design a dedicated block responsible for pre-processing signals obtained from sensors, preparing them for further processing in the processor. To achieve this goal, we have implemented a Simple Moving Average (SMA) filter as a pre-processing stage to effectively mitigate noise within the acquired sensor data. By employing this solution, not only can the noise be reduced, but also the power consumption is minimized. This is possible because the processor no longer needs to execute the noise reduction operation via software; instead, it can directly receive the pre-processed information from a low-power specialized block. Such an approach enables efficient signal conditioning while optimizing power efficiency in the overall system design.

II. Finite Impulse Response Filter and Simple Moving Average

A Finite Impulse Response (FIR) filter is a filter based on the FIR model, which is a model with exogenous inputs, and can be expressed by equation 1 [6]:

$$y(k) = b_1 u(k-1) + b_2 u(k-2) + \cdots + b_n u(k-n) \quad (1)$$

where u represents the input of the filter, and b_i are filter parameters. This type of filter operates by performing a weighted sum of n input samples, effectively functioning as a low-pass filter. It attenuates high-frequency components of the input signal and has diverse applications across several domains. [7] [8] [9] [10].

Simple Moving Average (SMA) is a particular case of FIR filters where all the parameters are the same and their sum is equal to 1. Equation 2 shows the mathematical model for this filter.

$$y(k) = \frac{u(k-1) + u(k-2) + u(k-3) + \cdots + u(k-n)}{n} \quad (2)$$

Although the SMA filter may lack the versatility of the FIR filter, it still holds practical value across many applications, as shown in [11], [12]. An example is the use of SMA filters with noise sensors to achieve more stable readings. In a study conducted by [13], various filters were analyzed and their effectiveness in noise reduction was assessed through simulations. The results indicated that the SMA filter was capable of reducing up to 95% of the noise. This finding suggests that the SMA filter performs well in mitigating high-frequency noise, making it a valuable tool for noise reduction tasks.

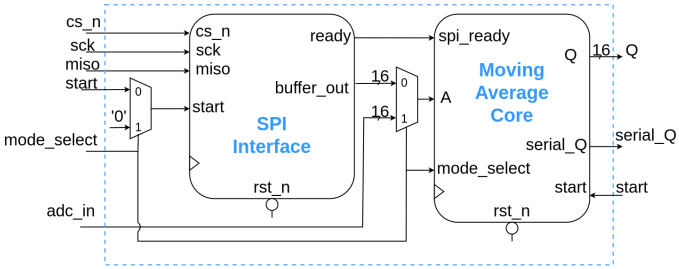

Fig. 2. Top level diagram of the module architecture.

III. Architecture

A. Top Level

The top level representation of the proposed architecture can be seen in Figure 2. The *SPI Interface* is responsible for providing a serial interface between a sensor and the *Moving Average Core*, which performs the SMA raw calculation.

The control input *mode_select* alternates between two modes. The first one uses the *SPI Interface* to communicate with the sensor, and the second one receives a raw 16-bit binary number in the *adc_in* input. The input *start* initiates the SMA calculation and the result can be shown in both outputs *Q* and its serial version *serial_Q*, in which the data can be serially sent to the UWB modulator.

B. Moving Average Core

In this architecture, the basic concept behind the SMA calculation is to compute it promptly upon the arrival of new data. An efficient approach is to use the previously calculated SMA values in the computation process. Then, the calculation of the SMA can be optimized, resulting in improved computational efficiency. From equation 2, we can write:

$$y(k) = \frac{u(k-1)}{n} + \frac{u(k-2) + u(k-3) + \cdots + u(k-n)}{n} \quad (3)$$

Equation 3 can be rewritten as:

$$y(k) = \frac{u(k-1)}{n} + \frac{u(k-2) + \cdots + u(k-n-1)}{n} - \frac{u(k-n-1)}{n} \quad (4)$$

Finally:

$$ny(k) = y(k-1) - u(k-n-1) + u(k-1) \quad (5)$$

By employing this definition, it becomes feasible to calculate the SMA using a single addition, a single subtraction, and a division operation. However, to further simplify this computation and optimize power and area usage, a shift operation can be employed to perform the division operation. While this approach may limit the flexibility of the architecture, it is highly effective in reducing power consumption and area requirements. For this particular case, Equation 5 can be expressed as follows:

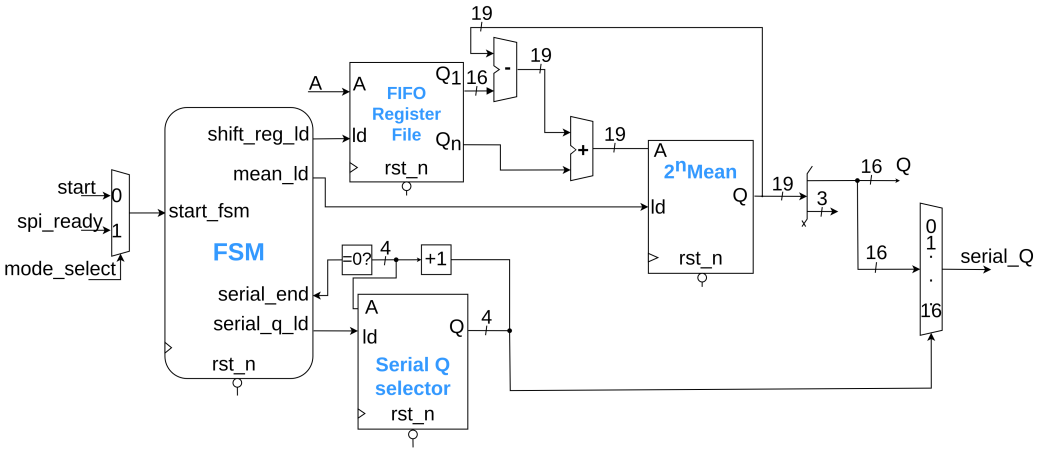

Fig. 3. Architecture of the moving average core.

$$2^n y(k) = y(k-1) - u(k-2^n-1) + u(k-1) \quad (6)$$

With equation 6, it is possible to compute the SMA using bit shifts. In the proposed architecture, the value of *n* will be set to 3, resulting in an SMA filter with 8 taps.

The proposed architecture of the *Moving Average Core* is depicted in Figure 3. It has a Finite State Machine (FSM) to control its operations and also a FIFO register file. In this block, the input labeled *A* is loaded into the first position of the FIFO when the *ld* input is activated. The output labeled *Q1* corresponds to the first position of the FIFO, which holds the first input read, while *Qn* represents the last position of the FIFO.

The subtractor and adder modules at the FIFO outputs are responsible for computing Equation 6, and the 19-bit result is registered in the $2^n Mean$ register. The next step is to perform a division by 2^n, which can be achieved by shifting the number to the left. This operation employs concatenation to discard the less significant bits, ensuring that the number is maintained as a 16-bit value and is shifted 3 times to the left.

A demultiplexer is used to serialize the SMA bits, so that they can be sent to the UWB transmitter. The serialization process is facilitated by the *Serial Q selector* register, which operates as a counter. Once the counter reaches its maximum value, it generates the *serial_end* signal, indicating to the FSM that the SMA calculation has reached its conclusion.

IV. Implementation and Results

The proposed architecture was implemented using 180 nm CMOS technology. The design was described in Verilog and the code was tested using a test vector with integer numbers between 0 and 4096, since the circuit works with 16 bit numbers. The results of the simulation are depicted in Figure 5. The dotted line represents the output of the circuit, while the solid line represents the input. This graph provides insight into the behavior of the filter and demonstrates its functionality.

Additionally, the result of the circuit is compared to a python model of a moving average, the comparison resulted in a 0.6125 average error. This is due to the fact that the circuit implements an integer division, which introduces an error, compared to a floating point implementation.

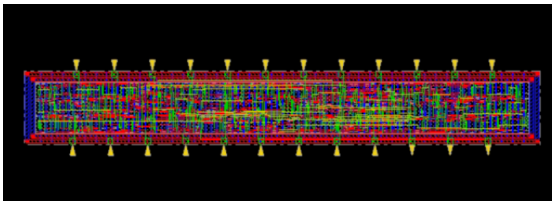

Fig. 4. Layout of the module implemented on CMOS 180nm technology.

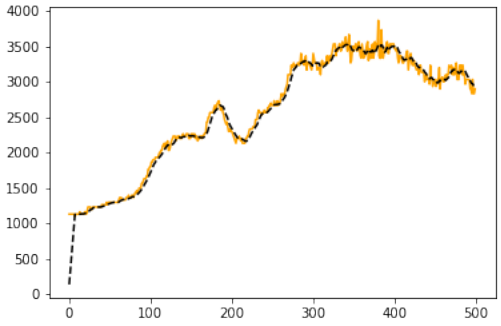

Fig. 5. Simulation of the moving average core.

Cadence tools were used for gate-level synthesis, as well as place and route steps. Simulations were conducted to gather data related to both area and power consumption and the resulting layout for the ASIC implementation is displayed in Figure 4.

An FPGA-based version was implemented for the circuit validation in hardware using the same Verilog code as the ASIC version, with some minimal adaptations. The power and resource consumptions were obtained with Vivado and the tests were performed on the Nexys 4 development board.

Table I presents the power consumption values of the ASIC implementation at five different frequencies, providing insights

TABLE I
POWER CONSUMPTION FOR DIFFERENT FREQUENCIES

	Internal Power	Switching Power	Leakage Power	Total Power
ASIC 1MHz	10.52 μW	2.58 μW	0.07 μW	13.17 μW
ASIC 750kHz	7.89 μW	1.93 μW	0.07 μW	9.89 μW
ASIC 500kHz	5.26 μW	1.29 μW	0.07 μW	6.62 μW
ASIC 250kHz	2.63 μW	0.64 μW	0.07 μW	3.34 μW
ASIC 125kHz	1.31 μW	0.32 μW	0.07 μW	1.71 μW
FPGA 1MHz	1000 μW		97000 μW	98000 μW

into the variation in dynamic power across them. In this case, the dynamic power consumption is higher compared to the total power consumed. For the FPGA case, most of the power consumed is due to the static power. The dynamic power in this scenario is relatively minimal, resulting in negligible variations in power consumption of the module with changes in frequency.

TABLE II
RESOURCES CONSUMPTION FOR FPGA PROTOTYPE

Resource	Utilization	Available	Utilization %
LUT	358	63400	0.17
LUTRAM	16	19000	0.08
FF	134	126800	0.11
IO	41	210	19.52

The utilization of the resources for the FPGA prototype can be seen in the Table II. The module demonstrates minimal resource usage, occupying less than 1% of the FPGA resources.

TABLE III
COMPARISON OF AREA AND POWER WITH FIR FILTER IMPLEMENTATIONS

	Taps	Technology	Area (μm^2)	Power (mW)
Aljuffri, 2015 (Sequential) [7]	8	LFoundry 150nm	30379	2.61
Aljuffri, 2015 (Parallel) [7]	8	LFoundry 150nm	58368	0.17
Annangi, 2017 [8]	144	Cadence 45nm	79220	20
Xu, 2013 [14]	16	SMIC 65nm	11335	1.30
Lou, 2017 [15]	36	CMOS 65nm	14810	4.43
Santos, 2023	8	UMC 180 nm	16758	0.013

Table III compares power and area consumption for different filter implementations with the proposed architecture in the end of the table. The proposed architecture differs from most of the implementations available in the literature by the utilization of a shift operation instead of a multiplier, leading to a simpler architecture. An example of architecture without multipliers is [15], this work implements a 36 tap filter achieving 4.43 mW. The power achieved by the proposed architecture is comparatively low compared to other architectures and have a low area consumption considering the technology used.

V. CONCLUSION

In this work, a dedicated Simple Moving Average filter was designed and implemented for the preprocessing stage of the DSP module within the Cedro Project, specifically for a UWB/UHF hybrid RFID tag. The SMA filter was prototyped in FPGA and the final ASIC version was sent for tape-out in October 2022. Simulation results validated the filter functionality and revealed that the module exhibits low power consumption in comparison to other FIR filter architectures suitable for this application.

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